IN THE CLAIMS:

All of the claims that remain pending and under consideration in the above-referenced application are presented, pursuant to 37 C.F.R. §§ 1.121(c)(1)(i) and 1.121(c)(3), in clean form below. Claim 21 is a newly submitted claim.

16. A method for forming an overlay target including a series of raised lines, the method comprising:

providing a substrate;

depositing a resist layer over said substrate;

patterning said resist layer to include a pattern defining said overlay target including a series of raised lines; and

etching said substrate to form said overlay target including a series of raised lines.

17. (Previously Amended) The method of claim 16, wherein said providing a substrate comprises providing a semiconductor substrate selected from a group consisting of silicon, gallium, and sapphire substrates.

18. (Previously Amended) The method of claim 17, wherein said depositing a resist layer over said substrate comprises depositing a resist layer directly over said semiconductor substrate selected from the group consisting of silicon, gallium, and sapphire substrates.

19. (Previously Amended) The method of claim 16, wherein said providing a substrate includes providing a semiconductor substrate having a top surface, a bottom surface, and a material layer deposited over said top surface.

20. (Previously Amended) The method of claim 19, wherein said depositing a resist layer over said substrate comprises depositing a resist layer over said material layer and said etching said substrate to form said overlay target including a series of raised lines comprises

--21. (New) The method of claim 16, wherein said etching comprises wet etching said substrate to form said overlay target including a series of raised lines.--